# *4 Stereo Inputs and 2 Channels Output Volume, Tone, Balance, Loudness and Selectable Input Gain*

## FEATURES

- Operation range : 2.7V~5V
- 4 stereo inputs with selectable input gain
- 2 independent speaker controls for balance
- Tone controls (treble and bass)
- Loudness and independent mute function
- Volume control in 1.25 dB/step
- $I^2C$ interface
- Components less and good PSRR
- Housed in SOP28, SSOP28 package

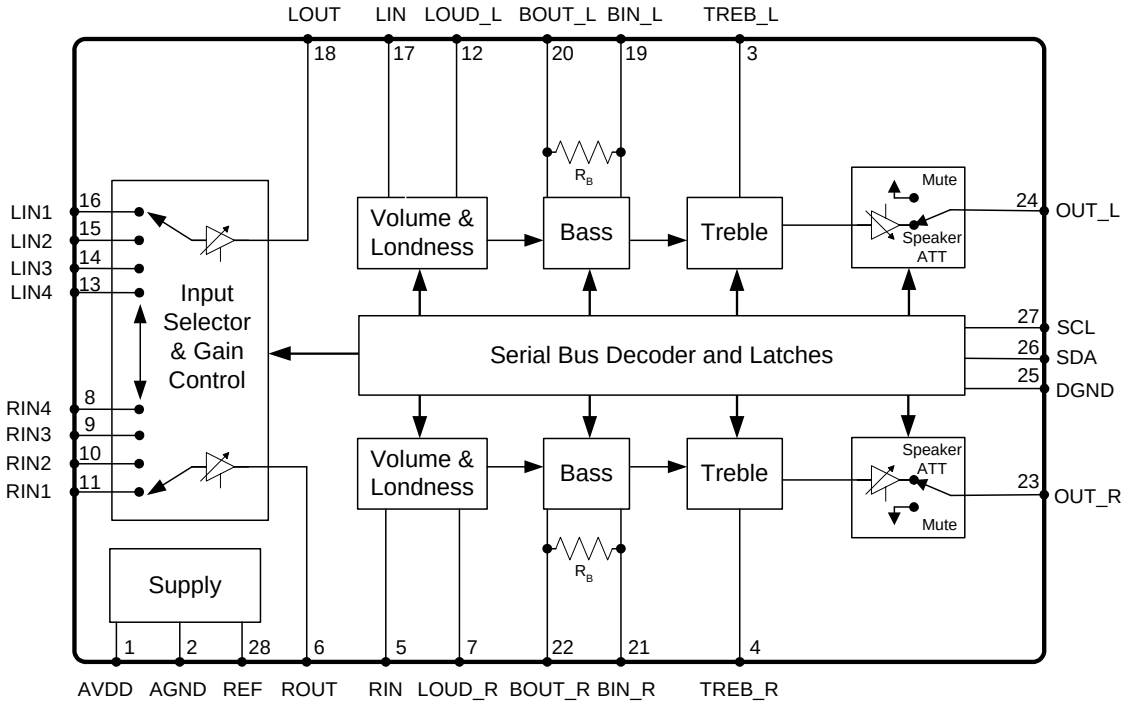
## APPLICATIONS

- Portable audio device
- Car stereo audio
- Hi-Fi audio system
- Cross-reference:
  PT2314

## DESCRIPTION

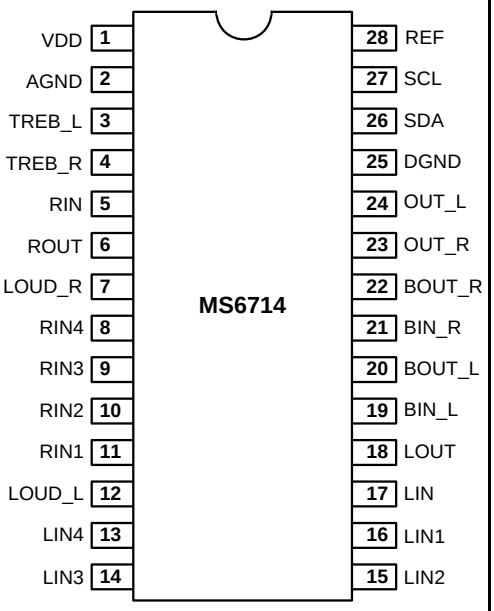
The MS6714 is a 4 stereo inputs/2-channel outputs digital control audio processor for the low voltage operation. Volume, tone (bass and treble), and balance (left/right) processor are incorporated into a single chip. The MS6714 also has the loudness function and selectable input gain. These functions can be built a Hi-Fi audio system easily. All functions are programmable via the serial $I^2C$ bus. The default states of the chip as the power is on are: the volume is -78.75dB, the stereo 4 is selected, all the speakers are mute and the gains of the input stage, the bass and the treble are 0dB.

## BLOCK DIAGRAM



## PIN CONFIGURATION

| Symbol | Pin | Description |
|---|---|---|
| VDD | 1 | Supply Input Voltage |
| AGND | 2 | Analog Ground |
| TREB_L | 3 | Left Channel Input for Treble Controller |
| TREB_R | 4 | Right Channel Input for Treble Controller |
| RIN | 5 | Audio Processor Right Channel Input |
| ROUT | 6 | Gain Output and Input Selector for Right Channel |
| LOUD_R | 7 | Right Channel Loudness Input |
| RIN4 | 8 | Right Channel Input 4 |
| RIN3 | 9 | Right Channel Input 3 |
| RIN2 | 10 | Right Channel Input 2 |
| RIN1 | 11 | Right Channel Input 1 |
| LOUD_L | 12 | Left Channel Loudness Input |
| LIN4 | 13 | Left Channel Input 4 |
| LIN3 | 14 | Left Channel Input 3 |
| LIN2 | 15 | Left Channel Input 2 |
| LIN1 | 16 | Left Channel Input 1 |
| LIN | 17 | Audio Processor Left Channel Input |
| LOUT | 18 | Gain Output and Input Selector for Left Channel |
| BIN_L | 19 | Left Bass Controller Input Channel |
| BOUT_L | 20 | Left Bass Controller Output Channel |
| BIN_R | 21 | Right Bass Controller Input Channel |
| BOUT_R | 22 | Right Bass Controller Output Channel |
| OUT_R | 23 | Right Speaker Output |
| OUT_L | 24 | Left Speaker Output |
| DGND | 25 | Digital Ground |
| SDA | 26 | $I^2C$ Data Input |
| SCL | 27 | $I^2C$ Clock Input |
| REF | 28 | Analog Reference Voltage（1/2VDD） |




**SOP28 / SSOP28**

## ORDERING INFORMATION

| Package | Part number | Packaging Marking | Transport Media |
|---|---|---|---|
| 28-Pin SOP (lead free) | MS6714GTR | MS6714G | 1k Units Tape and Reel |
| 28-Pin SOP (lead free) | MS6714GU | MS6714G | 25 Units Tube |
| 28-Pin SSOP (lead free) | MS6714SSGTR | MS6714G | 2.5k Units Tape and Reel |
| 28-Pin SSOP (lead free) | MS6714SSGU | MS6714G | 50 Units Tube |

## ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Rating | Unit |
|---|---|---|---|
| $V_{DD}$ | Supply Voltage | 6 | V |
| $V_{ESD}$ | Electrostatic Handling | -3000 to 3000 | V |
| $T_{STG}$ | Storage Temperature Range | -65 to 150 | ℃ |
| $T_A$ | Operating Ambient Temperature Range | -40 to 85 | ℃ |
| $T_J$ | Maximum Junction Temperature | 150 | ℃ |
| $T_S$ | Soldering Temperature, 10 seconds | 260 | ℃ |
| $R_{THJA}$ | Thermal Resistance from Junction to Ambient in Free Air<br>SOP28<br>SSOP28 | <br>210<br>210 | ℃/W |

## OPERATING RATINGS

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $V_{DD}$ | Supply Voltage | 2.7 | - | 5.5 | V |

## 5V ELECTRICAL CHARACTERISTICS

(Ta=25℃, All stages 0dB, f=1kHz, $C_{REF}$ =22uF, refer to the application circuit; unless otherwise specified)

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Supply** | | | | | | |
| $I_Q$ | Quiescent Current | $V_{IN}$=0V | - | 12.2 | 12.5 | mA |
| PSRR | Power Supply Rejection Ratio | $C_{REF}$ = 22uF, f = 100Hz | 55 | 60 | - | dB |
| **Input Selectors** | | | | | | |
| $R_{IN}$ | Input Resistance | Input 1,2,3,4 | 35 | 50 | 70 | kΩ |
| $G_{IN}$ | Input Gain Range | Gain | 0 | - | 11.25 | dB |
| $G_{STEP}$ | Step Resolution | | - | 3.75 | - | dB |
| $ERR_G$ | Gain Setting error | | -0.2 | 0 | 0.2 | dB |
| LOUD | Loudness | $C_{Loud}$=100nF, f =20Hz Volume=-40dB | 19 | 20 | - | dB |
| **Volume control** | | | | | | |
| $CR_{VOL}$ | Volume Control Range | Attenuation | -78.75 | - | 0 | dB |
| $RES_{VOL}$ | Volume Step Resolution | | - | 1.25 | - | dB |
| $ERR_{VOL}$ | Volume Setting Error | Av = 0 to -40dB | -1 | 0 | 0.5 | dB |
| | | Av = -40 to -60dB | -5 | 0 | 1 | dB |
| **Speaker Attenuators** | | | | | | |
| $CR_{SPK}$ | Speaker Control Range | Attenuation | -37.5 | - | 0 | dB |
| $RES_{SPK}$ | Speaker Step Resolution | | - | 1.25 | - | dB |
| $ERR_{SPK}$ | Speaker Setting Error | | -0.2 | 0 | 0.1 | dB |
| MUTE | Output Mute Attenuation | | - | -65 | -60 | dB |
| **Bass Control** | | | | | | |
| $CR_{BAS}$ | Bass Control Range | Boost/Cut | -14 | - | 14 | dB |
| $RES_{BAS}$ | Bass Step Resolution | | - | 2 | - | dB |
| $ERR_{BAS}$ | Speaker Setting Error | f =100Hz | -0.3 | 0 | 0.1 | dB |
| $R_B$ | Internal Feedback Resistance | | 34 | 44 | 58 | kΩ |
| **Treble Control** | | | | | | |
| $CR_{BAS}$ | Treble Control Range | Boost/Cut | -14 | - | 14 | dB |
| $RES_{BAS}$ | Treble Step Resolution | | - | 2 | - | dB |
| $ERR_{BAS}$ | Treble Setting Error | f =20kHz | -0.3 | 0 | 0.1 | dB |
| **General** | | | | | | |
| $VO_{MAX}$ | Maximum Output Voltage Swing | (THD+N)/S <0.3% | - | 4.5 | - | Vpp |
| THD+N | Total Harmonic Distortion Plus Noise | $V_{OUT}$=2Vpp | - | -75 | - | dB |
| | | | - | 0.0177 | - | % |
| S/N | Signal-to-Noise Ratio | $V_{OUT}$=4Vpp | - | 97 | - | dB |
| CS | Channel Separation Left/Right | | 93 | 97 | - | dB |
| **Bus Input** | | | | | | |
| $V_{IH}$ | Bus High Input Level | | 2 | - | - | V |
| $V_{IL}$ | Bus Low Input Level | | - | - | 0.8 | V |

Notes:
Bass and Treble response see to curve. The center frequency and quality of the response behavior can be chosen by the external.

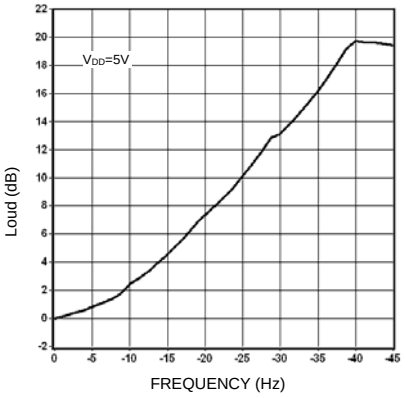
## 2.7V ELECTRICAL CHARACTERISTICS

(Ta=25℃, All stages 0dB, f=1kHz, $C_{REF}$ =22uF, refer to the application circuit; unless otherwise specified)

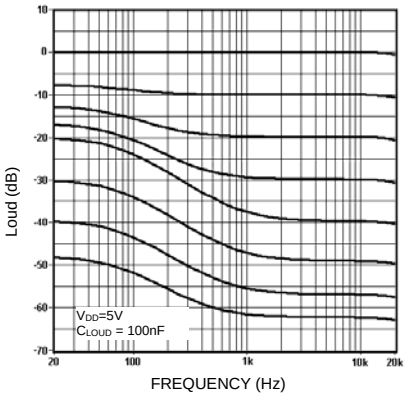
| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Supply** | | | | | | |
| $I_Q$ | Quiescent Current | $V_{IN}$=0V | - | 8.7 | 9 | mA |
| PSRR | Power Supply Rejection Ratio | $C_{REF}$ = 22uF, f = 100Hz | 53 | 58 | - | dB |
| **General** | | | | | | |
| $VO_{MAX}$ | Maximum Output Voltage Swing | (THD+N)/S <0.3% | - | 2.5 | - | Vpp |
| THD+N | Total Harmonic Distortion Plus Noise | $V_{OUT}$=2Vpp | - | -50 | - | dB |
| | | | - | 0.3 | - | % |
| S/N | Signal-to-Noise Ratio | $V_{OUT}$=2.5Vpp | 90 | 94 | - | dB |
| CS | Channel Separation Left/Right | | 90 | 94 | - | dB |

## TYPICAL PERFORMANCE CHARACTERISTICS

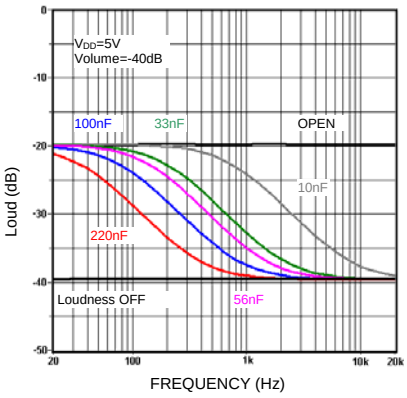
(Ta=25℃, All stages 0dB, f=1kHz, $C_{REF}$ =22uF, refer to the application circuit; unless otherwise specified)



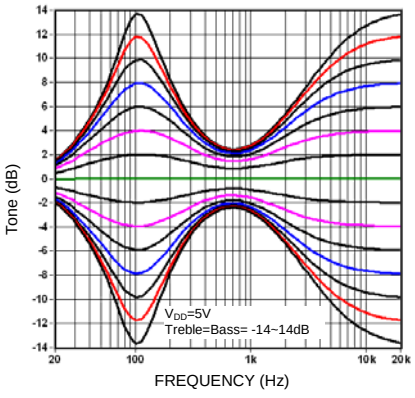

**Loudness vs. Volume**



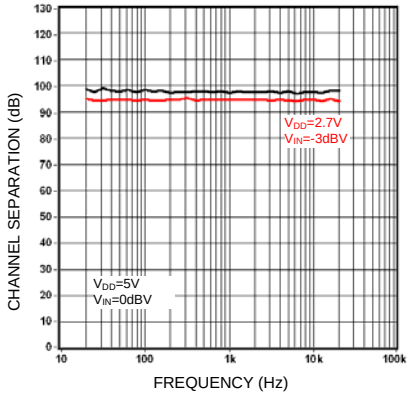

**Loudness vs. Frequency vs. Volume**



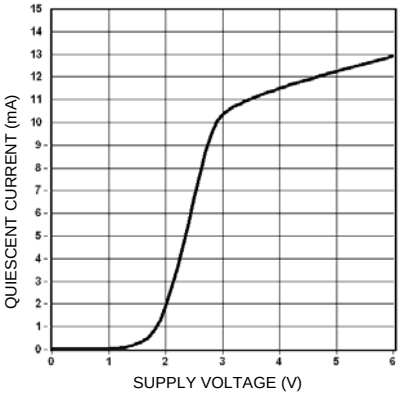

**Loudness vs. External Capacitors**



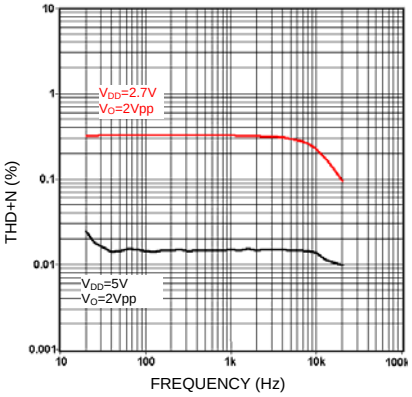

**Typical Tone Response**



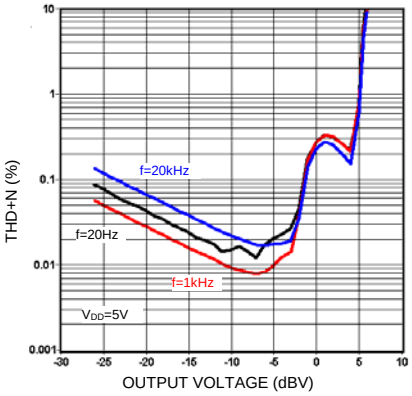

**Channel Separation vs. Frequency**



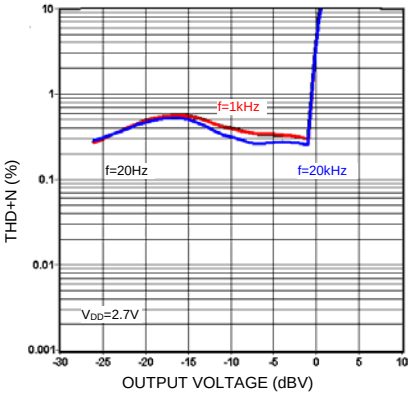

**Quiescent Current vs. Supply Voltage**



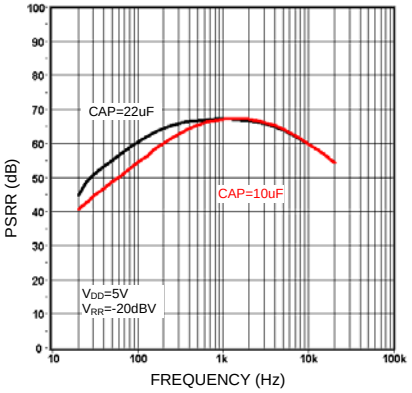

**THD+N vs. Frequency**



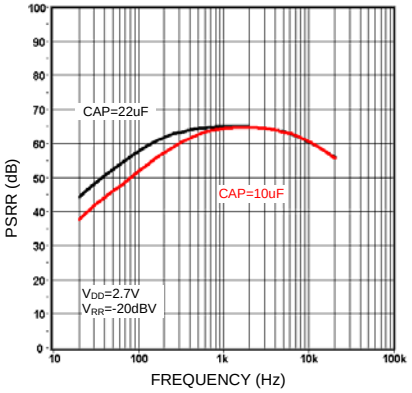

**THD+N vs. Output Voltage**




**THD+N vs. Output Voltage**




**PSRR vs. Frequency**

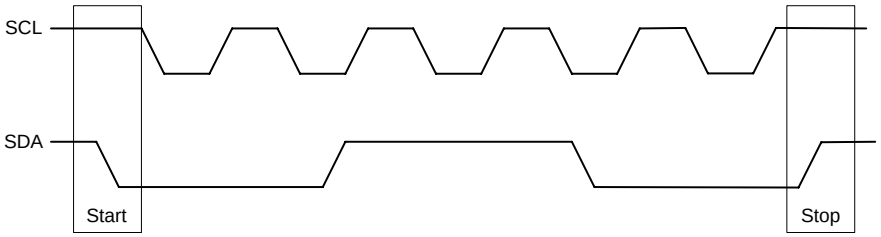



**PSRR vs. Frequency**

## I²C BUS DESCRIPTION

### Start and Stop Conditions

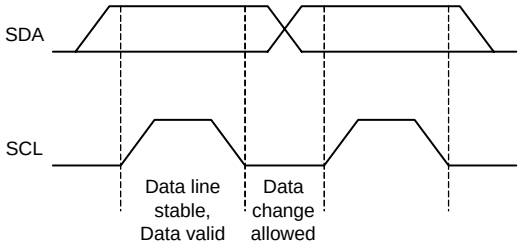
A start condition is activated when the SCL is set to HIGH and SDA shifts from HIGH to LOW state. The stop condition is activated when SCL is set to HIGH and SDA shifts from LOW to HIGH state. Please refer to the timing diagram below.




SCL : Serial Clock Line, SDA : Serial Data Line

### Data Validity

A data on the SDA line is considered valid and stable only when the SCL signal is in HIGH state. The HIGH and LOW states of the SDA line can only change when the SCL signal is LOW. Please refer to the figure below.

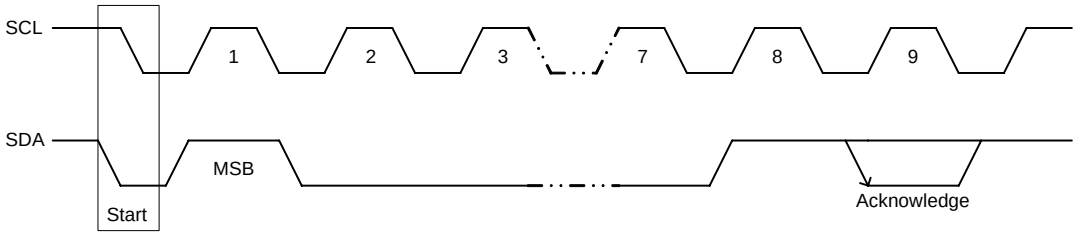



### Byte Format

Every byte transmitted to the SDA line consists of 8 bits. Each byte must be followed by an acknowledge bit. The MSB is transmitted first.

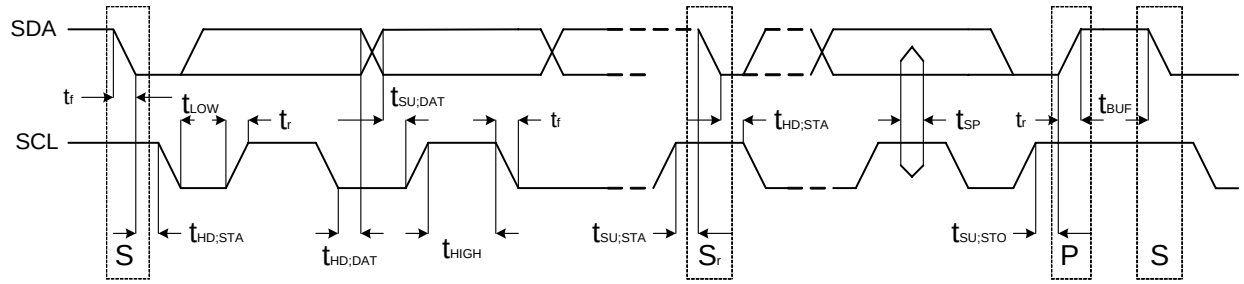
### Acknowledge

During the Acknowledge clock pulse, the master (up) put a resistive HIGH level on the SDA line. The peripheral (audio processor) that acknowledges has to pull-down (LOW) the SDA line during the Acknowledge clock pulse so that the SDA line is in a stable LOW state during this clock pulse. Please refer to the diagram below.




The audio processor that has been addressed has to generate an Acknowledge after receiving each byte, otherwise, the SDA line will remain at the HIGH level during the ninth (9th) clock pulse. In this case, the master transmitter can generate the STOP information in order to abort the transfer.

**Timing of SDA and SCL Bus Lines**

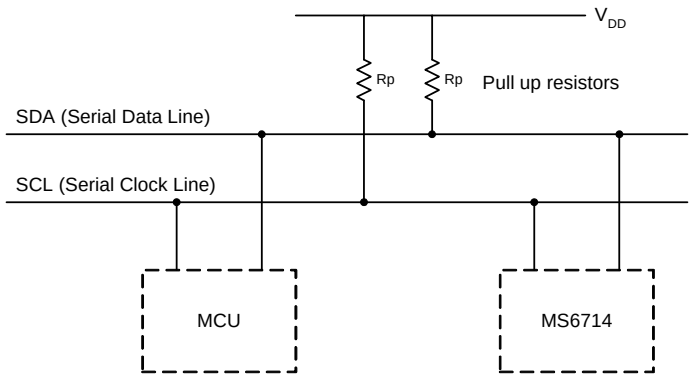



**Standard Mode**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $f_{SCL}$ | SCL clock frequency | 0 | 100 | kHz |
| $t_{HD:STA}$ | Hold time (repeated) START condition. After this period, the first clock pulse is generated | 4.0 | - | us |
| $t_{LOW}$ | LOW period of the SCL clock | 4.7 | - | us |
| $t_{HIGH}$ | HIGH period of the SCL clock | 4.0 | - | us |
| $t_{SU:STA}$ | Set-up time for a repeated START condition | 4.7 | - | us |
| $t_{HD:DAT}$ | Data hold time: For $I^2C$-bus devices | 0 | 3.45 | us |
| $t_{SU:DAT}$ | Data-set-up time | 250 | - | ns |
| $t_r$ | Rise time of both SDA and SCL signals | - | 1000 | ns |
| $t_f$ | Fall time of both SDA and SCL signals | - | 300 | ns |
| $t_{SU:STO}$ | Set-up time for STOP condition | 4.0 | - | us |
| $t_{BUF}$ | Bus free time between a STOP and START condition | 4.7 | - | us |
| $C_b$ | Capacitive load for each bus line | - | 400 | pF |
| $V_{nL}$ | Noise margin at the LOW level for each connected device (including hysteresis) | $0.1V_{DD}$ | - | V |
| $V_{nH}$ | Noise margin at the HIGH level for each connected device (including hysteresis) | $0.2V_{DD}$ | - | V |

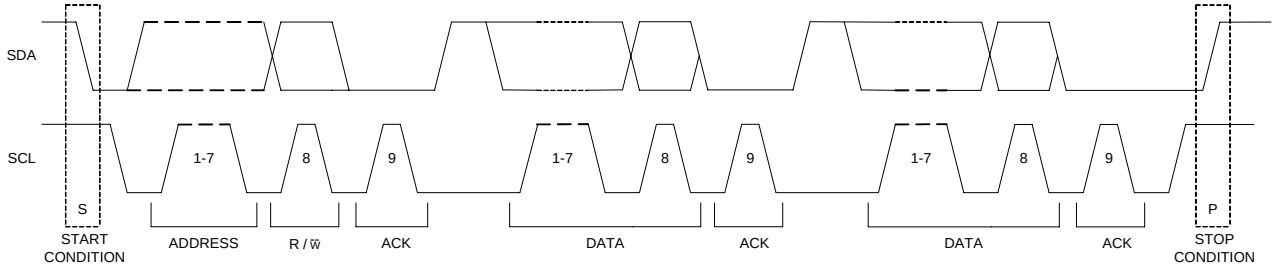
## BUS INTERFACE

Data are transmitted to and from the MCU to the MS6714 via the SDA and SCL. The SDA and SCL make up the BUS interface. It should be noted that pull-up resistors must be connected to the positive supply voltage.



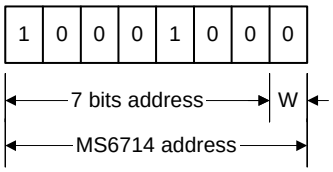
**Interface Protocol**

The format consists of the following
- A START condition
- A chip address byte including the MS6714 address. (7bits)
- The 8th bit of the byte must be "0".(write=0, read=1)
- MS6714 must always acknowledge the end of each transmitted byte.
- A data sequence (N-bytes + Acknowledge)
- A STOP condition




**Address Code**

The chip address of the MS6714 is 88H.




**Data Bytes Description**

The default states of the chip as the power is on are: the volume is -78.75dB, the stereo 4 is selected, all the speakers are mute and the gains of the input stage, the bass and the treble are 0dB.

| MSB | | | | | | | LSB | Function |
|---|---|---|---|---|---|---|---|---|
| 0 | 0 | B2 | B1 | B0 | A2 | A1 | A0 | Volume Control |
| 1 | 1 | 0 | B1 | B0 | A2 | A1 | A0 | Speaker ATT L |
| 1 | 1 | 1 | B1 | B0 | A2 | A1 | A0 | Speaker ATT R |
| 0 | 1 | 0 | G1 | G0 | S2 | S1 | S0 | Audio Switch |
| 0 | 1 | 1 | 0 | C3 | C2 | C1 | C0 | Bass Control |
| 0 | 1 | 1 | 1 | C3 | C2 | C1 | C0 | Treble Control |

Where Ax = 1.25dB steps; Bx = 10dB steps; Cx = 2dB steps; Gx = 3.75dB steps

**Volume**

| MSB | | | | | | | LSB | Function |
|---|---|---|---|---|---|---|---|---|
| **0** | **0** | **B2** | **B1** | **B0** | **A2** | **A1** | **A0** | **Volume 1.25 dB steps** |
| | | | | | 0 | 0 | 0 | 0 |
| | | | | | 0 | 0 | 1 | -1.25 |
| | | | | | 0 | 1 | 0 | -2.5 |
| | | | | | 0 | 1 | 1 | -3.75 |
| | | | | | 1 | 0 | 0 | -5 |
| | | | | | 1 | 0 | 1 | -6.25 |
| | | | | | 1 | 1 | 0 | -7.5 |
| | | | | | 1 | 1 | 1 | -8.75 |
| **0** | **0** | **B2** | **B1** | **B0** | **A2** | **A1** | **A0** | **Volume 10dB steps** |
| | | 0 | 0 | 0 | | | | 0 |
| | | 0 | 0 | 1 | | | | -10 |
| | | 0 | 1 | 0 | | | | -20 |
| | | 0 | 1 | 1 | | | | -30 |
| | | 1 | 0 | 0 | | | | -40 |
| | | 1 | 0 | 1 | | | | -50 |
| | | 1 | 1 | 0 | | | | -60 |
| | | 1 | 1 | 1 | | | | -70 |

The default volume is –78.75dB.

**Speaker Attenuator**

| MSB | | | | | | | LSB | Function（dB） |
|---|---|---|---|---|---|---|---|---|
| **1** | **1** | **0** | **B1** | **B0** | **A2** | **A1** | **A0** | **Speaker ATT L** |
| **1** | **1** | **1** | **B1** | **B0** | **A2** | **A1** | **A0** | **Speaker ATT R** |
| | | | | | 0 | 0 | 0 | 0 |
| | | | | | 0 | 0 | 1 | -1.25 |
| | | | | | 0 | 1 | 0 | -2.5 |
| | | | | | 0 | 1 | 1 | -3.75 |
| | | | | | 1 | 0 | 0 | -5 |
| | | | | | 1 | 0 | 1 | -6.25 |
| | | | | | 1 | 1 | 0 | -7.5 |
| | | | | | 1 | 1 | 1 | -8.75 |
| | | | 0 | 0 | | | | 0 |
| | | | 0 | 1 | | | | -10 |
| | | | 1 | 0 | | | | -20 |
| | | | 1 | 1 | | | | -30 |
| | | | 1 | 1 | 1 | 1 | 1 | Mute |

LF: Left Front, RF: Right Front, LR: Left Rear, RR: Right Rear
The default state is mute.

**Audio Switch**

| MSB | | | | | | | LSB | Function |
|---|---|---|---|---|---|---|---|---|
| **0** | **1** | **0** | **G1** | **G0** | **S2** | **S1** | **S0** | **Audio Switch** |
| | | | | | | 0 | 0 | Stereo 1 |
| | | | | | | 0 | 1 | Stereo 2 |
| | | | | | | 1 | 0 | Stereo 3 |
| | | | | | | 1 | 1 | Stereo 4 |
| | | | | | 0 | | | Loudness ON |
| | | | | | 1 | | | Loudness OFF |
| | | | 0 | 0 | | | | +11.25dB |
| | | | 0 | 1 | | | | +7.5dB |
| | | | 1 | 0 | | | | +3.75dB |
| | | | 1 | 1 | | | | 0dB |

The default state is stereo 4, loudness off and gain 0dB.

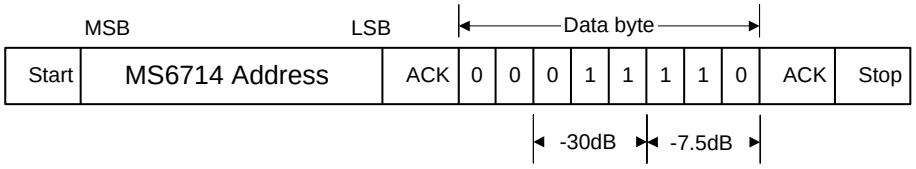
**Bass and Treble**

| MSB | | | | | | | LSB | Function（dB） |
|---|---|---|---|---|---|---|---|---|
| **0** | **1** | **1** | **0** | **C3** | **C2** | **C1** | **C0** | **Bass** |
| **0** | **1** | **1** | **1** | **C3** | **C2** | **C1** | **C0** | **Treble** |
| | | | | 0 | 0 | 0 | 0 | -14 |
| | | | | 0 | 0 | 0 | 1 | -12 |
| | | | | 0 | 0 | 1 | 0 | -10 |
| | | | | 0 | 0 | 1 | 1 | -8 |
| | | | | 0 | 1 | 0 | 0 | -6 |
| | | | | 0 | 1 | 0 | 1 | -4 |
| | | | | 0 | 1 | 1 | 0 | -2 |
| | | | | 0 | 1 | 1 | 1 | 0 |
| | | | | 1 | 0 | 0 | 0 | 0 |
| | | | | 1 | 0 | 0 | 1 | 2 |
| | | | | 1 | 0 | 1 | 0 | 4 |
| | | | | 1 | 0 | 1 | 1 | 6 |
| | | | | 1 | 1 | 0 | 0 | 8 |
| | | | | 1 | 1 | 0 | 1 | 10 |
| | | | | 1 | 1 | 1 | 0 | 12 |
| | | | | 1 | 1 | 1 | 1 | 14 |

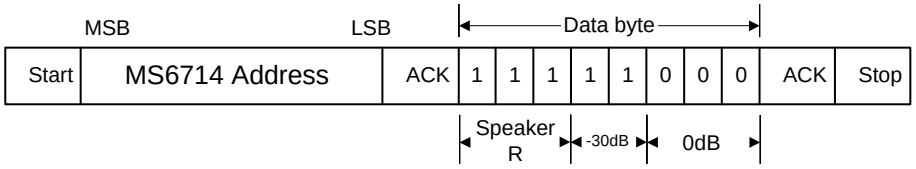
The default state is bass 0dB and treble 0dB.

**Examples**

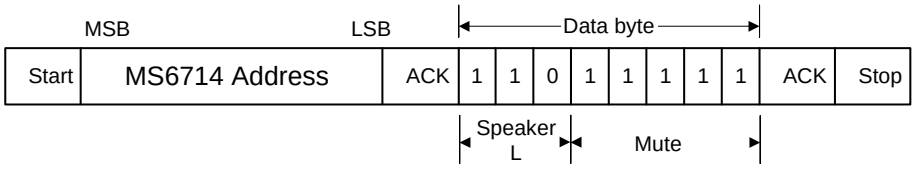
Set Volume at –37.5dB.



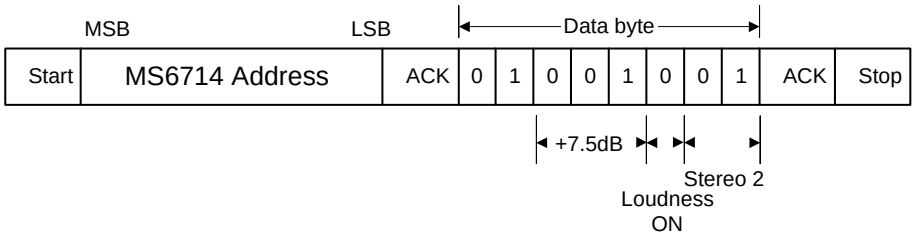

Set Speaker Right at –30dB.



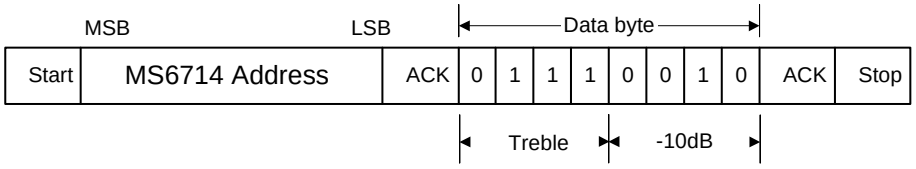

Set Speaker Left in mute-on.




Set Stereo 2 Input with gain of +7.5 dB and Loudness on.

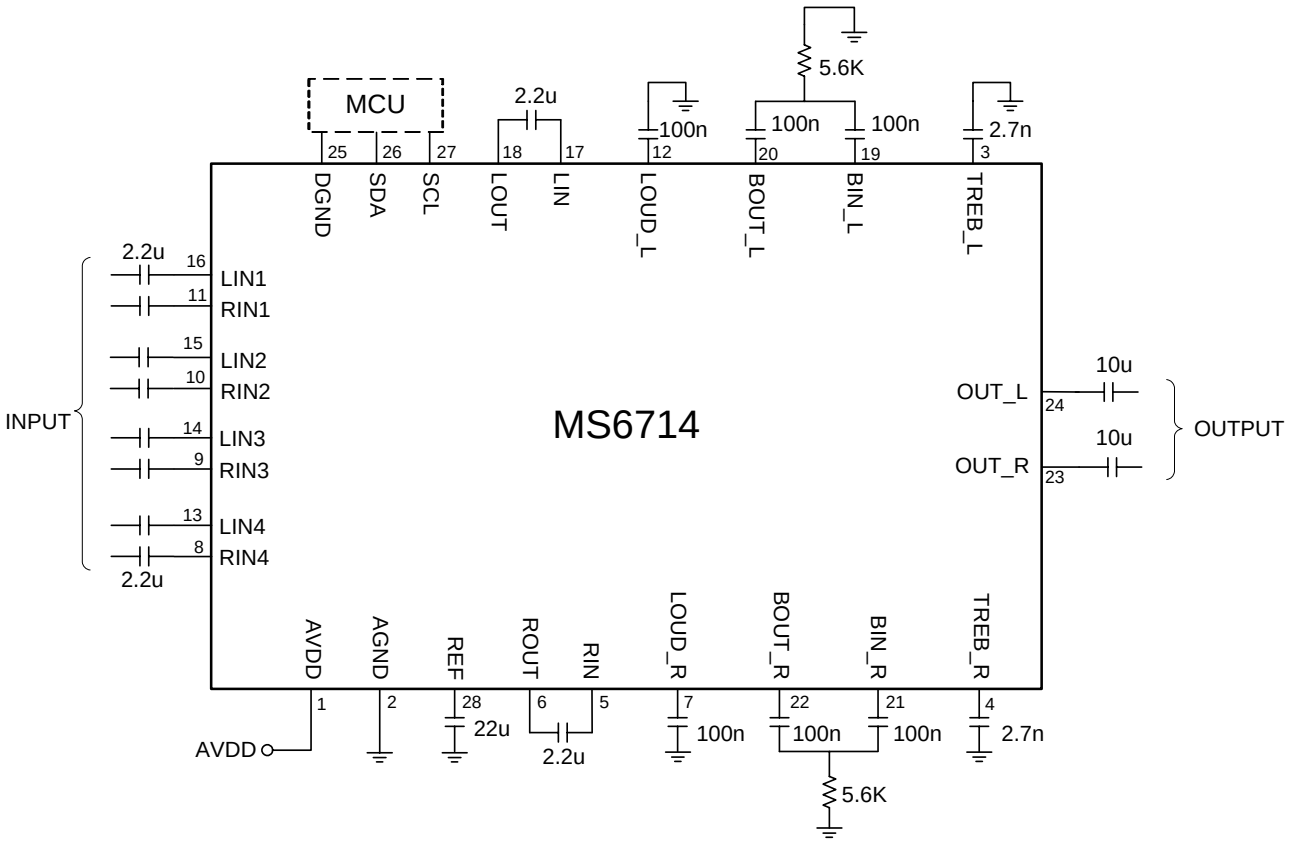



Set treble at -10dB.



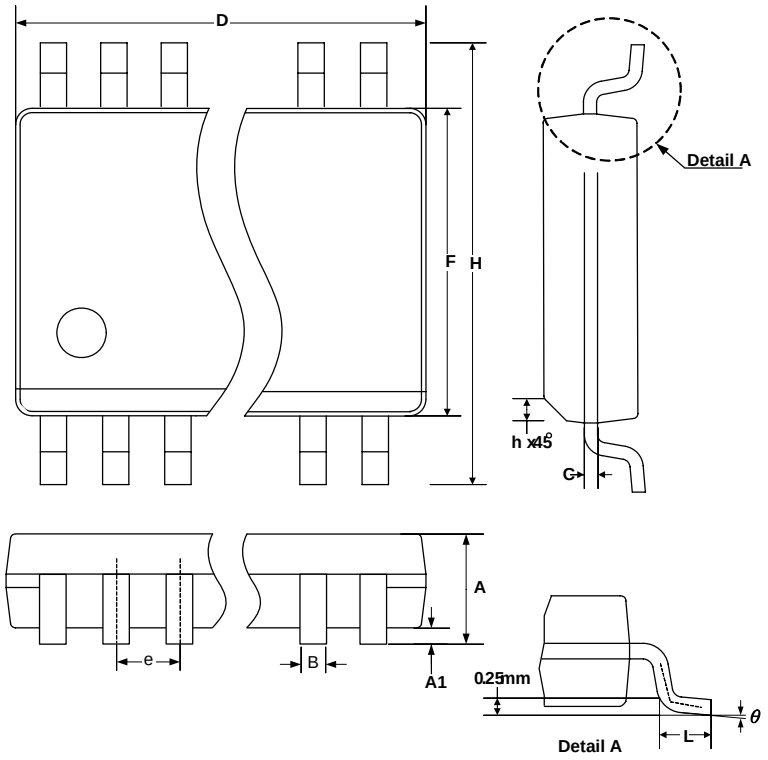
## APPLICATION INFORMATION

**Basic Application Example**



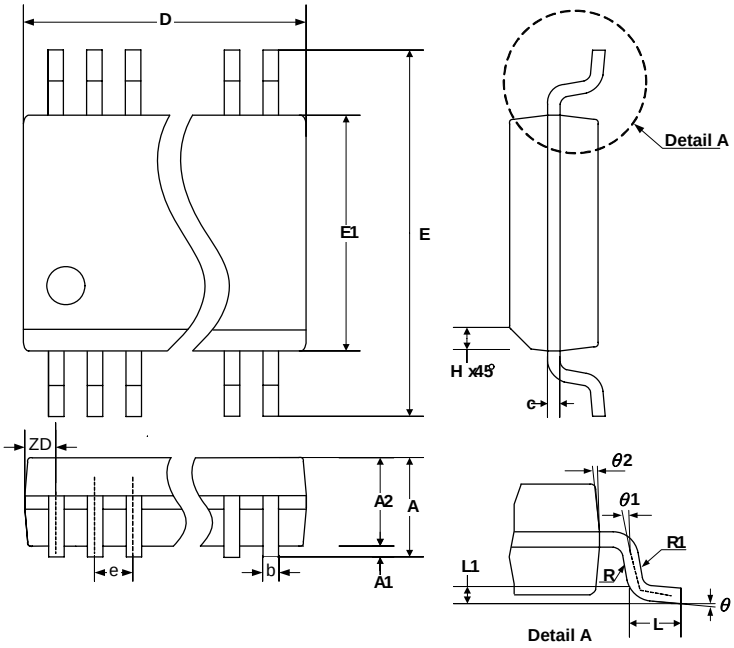
## EXTERNAL DIMENSIONS

### SOP28 (300mil)




| Symbol | Dimension in mm | | Dimension in inch | |
|---|---|---|---|---|
| | Min | Max | Min | Max |
| A | 2.35 | 2.65 | 0.0926 | 0.1043 |
| A1 | 0.10 | 0.30 | 0.0040 | 0.0118 |
| B | 0.33 | 0.51 | 0.013 | 0.020 |
| C | 0.23 | 0.32 | 0.0091 | 0.0125 |
| e | 1.27 BASIC | | 0.050 BASIC | |
| E | 7.40 | 7.60 | 0.2914 | 0.2992 |
| H | 10.00 | 10.65 | 0.394 | 0.419 |
| L | 0.40 | 1.27 | 0.016 | 0.050 |
| D | 17.70 | 18.10 | 0.6969 | 0.7125 |
| h | 0.25 | 0.75 | 0.010 | 0.029 |
| $\theta$ | $0^o$ | $8^o$ | $0^o$ | $8^o$ |

**SSOP28**




| Symbol | Dimension in mm | | | Dimension in inch | | |
|---|---|---|---|---|---|---|
| | Min | NOM | Max | Min | NOM | Max |
| A | 1.35 | 1.63 | 1.75 | 0.053 | 0.064 | 0.069 |
| A1 | 0.10 | 0.15 | 0.25 | 0.004 | 0.006 | 0.010 |
| A2 | - | - | 1.50 | - | - | 0.059 |
| b | 0.20 | - | 0.30 | 0.008 | - | 0.012 |
| c | 0.18 | - | 0.25 | 0.007 | - | 0.010 |
| e | 0.635 BASIC | | | 0.025 BASIC | | |
| D | 8.56 | 9.91 | 8.74 | 0.337 | 0.390 | 0.344 |
| E | 5.79 | 5.99 | 6.20 | 0.228 | 0.236 | 0.244 |
| E1 | 3.81 | 3.91 | 3.99 | 0.150 | 0.154 | 0.157 |
| L | 0.41 | 0.635 | 1.27 | 0.016 | 0.025 | 0.050 |
| h | 0.25 | - | 0.50 | 0.010 | - | 0.020 |
| ZD | 0.838REF | | | 0.033REF | | |
| R1 | 0.20 | - | 0.33 | 0.008 | - | 0.013 |
| R | 0.20 | - | - | 0.008 | - | - |
| $\theta$ | $0^o$ | - | $8^o$ | $0^o$ | - | $8^o$ |
| $\theta$ 1 | $0^o$ | - | | $-0^o$ | - | - |
| $\theta$ 2 | $5^o$ | $10^o$ | $15^o$ | $5^o$ | $10^o$ | $15^o$ |